WHAT IS CLAIMED IS:

1. A device comprising:

a synchronization circuit to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal, and to generate a load signal based on the synchronized synchronization signal; and

a ring counter to receive the load signal from the synchronization circuit and to circularly propagate the load signal.

2. A device according to Claim 1, further comprising:

an enabling circuit to assert and to deassert an enable signal,

wherein the ring counter is to receive the enable signal, to receive the load signal from the synchronization circuit if the enable signal is asserted, and to circularly propagate the load signal if the enable signal is deasserted.

3. A device according to Claim 2, wherein the enabling circuit comprises

a circuit to detect whether a load pulse within the load signal has been received by the ring counter, and to deassert the enable signal if the load pulse has been received by the ring counter.

4. A device according to Claim 1, wherein the ring counter comprises:

one or more delay elements to receive the load signal, to delay the load signal, and to output the delayed load signal.

5. A device according to Claim 4, the clock signal to reflect a clock period, and each of the one or more delay elements to delay the load signal for a respective period substantially equal to an integer multiple of the clock period.

6. A device according to Claim 4, further comprising:

a multiplexer to receive a delayed load signal from a plurality of the one or more delay elements, to receive an offset signal, and to output one of the received delayed load signals based on the offset signal.

7. A device according to Claim 1, further comprising:

a multiplexer to receive the load signal from the synchronization circuit, to receive a circularly propagating load signal from the ring counter, to receive an enable signal, to output the received load signal to the ring counter if the enable signal is asserted, and to output the circularly propagating load signal to the ring counter if the enable signal is deasserted.

8. A device according to Claim 7, further comprising:

an enabling circuit to detect whether a load pulse of the load signal has been received by the ring counter, and to deassert the enable signal only if the load pulse has been received by the ring counter.

9. A device according to Claim 1, wherein the synchronization circuit comprises:

a delay element to delay the synchronized synchronization signal;

an inverter to invert the delayed synchronized synchronization signal; and

a logic element to AND the delayed inverted signal and the synchronized synchronization signal, and to output the load signal.

10. A method comprising:

receiving a synchronization signal, the synchronization signal substantially synchronized with a data transition;

synchronizing the synchronization signal with a clock signal;

generating a load signal based on the synchronized synchronization signal, the load signal including a load pulse;

inputting the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to a minimum data transition period; and

outputting the load signal from a first node of the ring counter, a period between successive outputs of the load pulse being substantially equal to the data transition period.

11. A method according to Claim 10, wherein the synchronization signal is synchronized with a data signal, the data signal reflecting the minimum data transition period.

12. A method according to Claim 11, wherein the period of the synchronization signal is substantially equal to the data transition period.

13. A method according to Claim 10, wherein generating the load signal comprises:

delaying the synchronized synchronization signal;

inverting the delayed synchronized synchronization signal; and

performing a logical AND operation on the delayed inverted signal and the synchronized synchronization signal to generate the load signal.

14. A method according to Claim 13, wherein the inverted signal is delayed by one period of the clock signal.

15. A method according to Claim 10, wherein outputting the load signal from the ring counter comprises:

receiving a plurality of load signals from the ring counter, at least one of the plurality of load signals being delayed with respect to at least one other of the plurality of load signals;

selecting one of the plurality of load signals to output; and

outputting the selected load signal.

16. A method according to Claim 15, wherein a load pulse of the selected load signal is substantially synchronized with a center of the data eye.

17. A method according to Claim 15, wherein selecting one of the plurality of load signals comprises:

receiving an offset signal;

selecting a load signal output from one of the one or more delay elements based on the offset signal.

18. A method according to Claim 10, wherein inputting the load signal comprises:

asserting an enable signal to input the load signal into the ring counter, and further comprising:

deasserting the enable signal to shift the load signal through the ring counter.

19. A device to:

receive a synchronization signal, the synchronization signal substantially synchronized with a minimum data transition period;

synchronize the synchronization signal with a clock signal;

generate a load signal based on the synchronized synchronization signal, the load signal including a load pulse;

input the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to the minimum data transition period; and

output the load signal from a first node of the ring counter, a period between successive outputs of the load pulse being substantially equal to the minimum data transition period.

20. A device according to Claim 19, the synchronization signal to be synchronized with a data signal, the data signal to reflect the minimum data transition period.

21. A device according to Claim 20, the period of the synchronization signal to be substantially equal to the data transition period.

22. A device according to Claim 19, wherein generation of the load signal comprises:

delay of the synchronized synchronization signal;

inversion of the delayed synchronized synchronization signal; and

performance of a logical AND operation on the delayed inverted signal and the synchronized synchronization signal to generate the load signal.

23. A device according to Claim 22, the inverted signal to be delayed by one period of the clock signal.

24. A device according to Claim 19., wherein output of the load signal from the ring counter comprises:

reception of a plurality of load signals from the ring counter, at least one of the plurality of load signals to be delayed with respect to at least one other of the plurality of load signals;

selection of one of the plurality of load signals to output; and

output of the selected load signal.

25. A device according to Claim 24, wherein a load pulse of the selected load signal is to be substantially synchronized with a center of the data eye.

26. A device according to Claim 24, wherein selection of one of the plurality of load signals comprises:

reception of an offset signal;

selection of a load signal output from one of the one or more delay elements based on the offset signal.

27. A device according to Claim 19, wherein input of the load pulse comprises:

assertion of an enable signal to input the load signal into the ring counter, and

the device further to:

deassert the enable signal to shift the load signal through the ring counter.

28. A system comprising:

a memory controller hub comprising:

a synchronization circuit to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal, and to generate a load signal based on the synchronized synchronization signal;

a ring counter to receive the load signal from the synchronization circuit and to circularly propagate the load signal; and

a parallel-to-serial converter to generate serial data based on the load signal; and

a double data rate memory to receive the serial data.

29. A system according to Claim 28, wherein the ring counter comprises one or more delay elements to receive the load signal, to delay the load signal, and to output the delayed load signal, and

wherein the memory controller hub further comprises a multiplexer to receive a delayed load signal from a plurality of the one or more delay elements, to receive an offset signal, and to output one of the received delayed load signals based on the offset signal.